Remarks

Applicant respectfully request reconsideration of this application as amended. Claims 1, 8, 11-13, 16 and 25 have been amended. Claims 4, 5 and 15 have been cancelled. Therefore, claims 1-3, 6-14 and 16-27 are presented for examination.

Claim 10 stands rejected under 35 U.S.C. §112, second paragraph. Applicant submits that the claims have been amended to appear in proper condition for allowance.

Claims 1-5, 7, 9, 10-19, 20 and 22-24 stand rejected under 35 U.S.C. §102(e) as being anticipated by Horvitz (U.S. Patent No. 6,009,452). Further, claim 21 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Horvitz. Applicant submits that the present claims are patentable over Horvitz.

Horvitz discloses that a task instance is selected at a beginning of each of idle-time intervals and processed during the remainder of that interval. The selected instance is one that is most likely to occur in the near-future and will be precomputed, during an associated idle-time interval, to the extent of the remaining time available during that interval. Once this task instance has been precomputed, its results, partial if the task has not completed prior to the end of the interval, are stored for subsequent access and use. Ideally, by having these results precomputed and ready for future use, future response time, i.e. run-time delay, is appreciably shortened since that task instance, when it would otherwise be dispatched for execution, will have already executed--fully or at least partially. In this manner, available computer resources, here processing time, are maintained at relatively high usage during all time periods, rather than experiencing bursty usage patterns as conventionally occurs; hence, significantly enhancing overall system throughput. See Horvitz at col. 9, ll. 39-57

Claim 1 of the present application recites examining an instruction stream of a non-executing thread during execution of an executing thread, determining whether the hardware resource is available to the instruction of the non-executing thread and enabling execution of the non-executing thread if the hardware resource is available to the instruction of the non-executing thread. Applicant submits that Horvitz does not disclose or suggest a process of *examining an instruction stream of a non-executing thread **during execution of an executing thread** and enabling execution of the non-executing thread if a hardware resource is available to the instruction of the non-executing thread.*

In fact, Horvitz discloses selecting a task instance at the beginning of idle-time intervals and processing them during the remainder of that interval. Thus, Horvitz teaches away from a process of *examining an instruction stream of a non-executing thread **during execution of an executing thread***. As a result, claim 1 is patentable over Horvitz.

Independent claims 13, 16 and 25 include features similar to those recited in claim 1. Thus claims 13, 16 and 25, and their respective dependent claims, are patentable over Horvitz for reasons similar to those recited in claim 1.

Claims 6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Horvitz (U.S. Patent No. 6,009,452) in view of Budde et al. (U.S. Patent No. 4,891,753). Applicant submits that the present claims are patentable over Horvitz even in view of Budde.

Budde discloses register scorboarding on a microprocessor chip. Nonetheless, Budde does not disclose or suggest examining an instruction stream of a non-executing thread during execution of an executing thread, determining whether the hardware resource is available to the instruction of the non-executing thread and enabling execution of the non-executing thread if the hardware resource is available to the instruction of the non-executing

thread. As discussed above, Horvitz does not disclose or suggest such a feature. Therefore, the combination of Horvitz and Budde would not disclose the feature. Accordingly, the present claims are patentable over Horvitz in view of Budde.

Claims 25, 26 and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Horvitz in view of Dukach et al. (U.S. Publication No. 2004/0036622). Applicant submits that the present claims are patentable over Horvitz even in view of Dukach.

Dukach discloses a system that shows messages on electronic displays, including networks of outdoor displays, such as displays mounted on vehicles. See Dukach at Abstract. However, Dukach does not disclose or suggest examining an instruction stream of a non-executing thread during execution of an executing thread, determining whether the hardware resource is available to the instruction of the non-executing thread and enabling execution of the non-executing thread if the hardware resource is available to the instruction of the non-executing thread. As discussed above, Horvitz does not disclose or suggest such a feature. Therefore, the combination of Horvitz and Dukach would not disclose the feature. Accordingly, the present claims are patentable over Horvitz in view of Dukach.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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